EUV Lithography at the 22-nm technology node

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ABSTRACT

We are evaluating the readiness of extreme ultraviolet (EUV) lithography for insertion into production at the 15 nm technology node by integrating it into standard semiconductor process flows because we believe that device integration exercises provide the truest test of technology readiness and, at the same time, highlight the remaining critical issues. In this paper, we describe the use of EUV lithography with the 0.25 NA Alpha Demo Tool (ADT) to pattern the contact and first interconnect levels of a large (~24 mm x 32 mm) 22 nm node test chip using EUV masks with state-of-the-art defectivity (~0.3 defects/cm^2). We have found that: 1) the quality of EUVL printing at the 22 nm node is considerably higher than the printing produced with 193 nm immersion lithography; 2) printing at the 22 nm node with EUV lithography results in higher yield than double exposure double-etch 193i lithography; and 3) EUV lithography with the 0.25 NA ADT is capable of supporting some early device development work at the 15 nm technology node.

Keywords: Extreme ultraviolet lithography, EUVL, EUV device integration, EUV OPC, EUV mask, EUV resist process

1. INTRODUCTION

Extreme ultraviolet (EUV) lithography is beginning to prove useful for the patterning of the most difficult layers in SRAM device scaling work (contact and first interconnect levels). Early in 2008, the EUV Alpha Demo Tool (ADT) in Albany, New York was used to pattern the first interconnect level of 45-nm node test chips[1] manufactured at AMD's fabrication facility in Dresden, Germany. Later in 2008, electrical functioning 0.186 µm^2 FinFET-based 6T-SRAM cells in 32-nm node test chips were demonstrated using EUV and 193 nm immersion lithography[2] at IMEC in Leuven, Belgium. Early in 2009, the EUV ADT in Albany was used to pattern the contact and first interconnect levels of 0.08 µm^2 6T-SRAM cells in small (~5.5 mm x ~10.5 mm) 22-nm node test chips.[3] In this paper, we describe the patterning of one critical layer in 0.076 µm^2 and 0.094 µm^2 SRAM cells in large (~24 mm x ~32 mm) 22-nm node test chips with single exposure EUV lithography; the other layers were patterned with double-dipole or double-exposure double-etch 193 nm immersion lithography. In Section 2, we describe EUV data correction for a contact level mask, report on CD control, resist process window, and contact to active overlay (EUV lithography to 193 immersion lithography) using

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EUV lithography, summarize the processing steps that take place after EUV lithography, and provide butterfly curves for electrically-active 0.076 μm^2 SRAM fly cells. In Section 3, we present descriptions of EUV data correction for an interconnect level mask, describe EUV patterning of the first interconnect level of 22-nm node test chips, and provide butterfly curves for 0.094 μm^2 SRAM flycells. In Section 4, we show that the 0.25 NA EUV ADT is capable of supporting some early device development at the 15 nm technology node and present some EUV imaging results of interconnect SRAM patterns scaled from 80 nm pitch to 56 nm pitch that were printed with and without the use of optical proximity corrections to the mask layout. Our conclusions are presented in Section 5.

2. 22-nm NODE TEST CHIPS WITH EUVL CONTACT LEVEL

The layer structure of the 22-nm node test chip used in the EUV device demonstration work described in this section, in which the contact (CA) level was patterned with single exposure EUV lithography and the first interconnect (M1) level was patterned with double-dipole (DDL)[4] 193 nm immersion lithography, is illustrated in Figure 1. The chip employs high-κ metal gate FinFET transistors[5] with 25 nm gate length on silicon-on-insulator (SOI) substrates fabricated using 193 nm immersion lithography. Fin formation was carried out using a double-exposure, double-etch (DE^2) sidewall image transfer (SIT) process. The metal gate electrodes were patterned using DE^2 193 nm immersion lithography.[6]

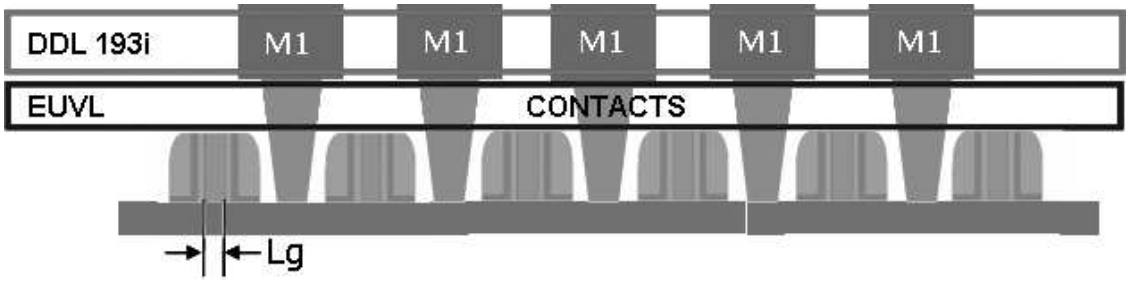


Figure 1 – Integrated stack for 22-nm node test chip in which the contact level was patterned using single exposure EUV lithography and the first interconnect (M1) level was patterned using double-dipole 193 immersion lithography.

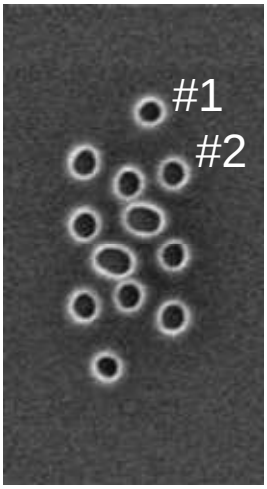
The data for the 22-nm contact level EUV mask was corrected for conventional optical proximity correction (OPC) and for mask shadowing, but not for imaging system flare because the pattern density at the contact level is quite small (~6%). Model-based OPC was applied to the layout data using Mentor Graphics Calibre nmOPC[7] using the following inputs: 0.25 numerical aperture (NA) imaging system with a centroid wavelength of 13.5 nm and illuminated with fixed conventional illumination with partial coherence of 0.5. A simple threshold model was used for the resist; resist blur due to acid diffusion was assumed to be 20 nm. The contact level data was corrected for the mask shadow effect by modifying square contact holes so that their vertical dimension was 0.95 nm larger and their horizontal dimension was 1.9 nm smaller. The corrected data was used by the Advanced Mask Technology Center (AMTC) in Dresden, Germany to fabricate a contact level EUV mask on a ULE 6025 blank with a 2.5 nm thick Ru-capped MoSi multilayer reflector, a 10 nm CrN buffer layer, and a 70 nm thick TaBN absorber. KLA-Tencor 5xx inspection of the completed mask located 34 defects > 60 nm in size, which corresponds to a defect density of ~ 0.3 defects/cm^2.

EUV lithography at the contact level was carried out using the 0.25 NA EUV ADT[8] in Albany, New York. The resist used for contact level patterning was SEVR-78 and is available from Shin-Etsu MicroSci, Inc. The process latitude and other relevant performance parameters for SEVR-78 resist when printing a dense array of 40 nm diameter contact holes in a 100 nm thick film using the ADT is shown in Figure 2.

Exposure Latitude	DOF (nm)	Dose (mJ/cm^2)	CDU (nm)	Circularity	Eccentricity
33.9%	~200	18	4.7	1.03	0.35

Figure 2 – Data on exposure latitude, depth of focus, circularity, and eccentricity when printing a dense array of 40 nm diameter contact holes in 100 nm thick films of SEVR 78 resist at 18 mJ/cm^2 dose.

The quality of the contact holes images in 100 nm thick films of SEVR 78 resist is illustrated in Figure 3, which shows a top-down SEM image of the contact level of a 0.076 μm^2 6T-SRAM flycell. Surprisingly, the ~ 20 nm spaces between the pairs of closely spaced contacts in the center of the flycell pattern were consistently resolved. The average CD and variation for two specific contact holes in the pattern is also provided in Figure 3.



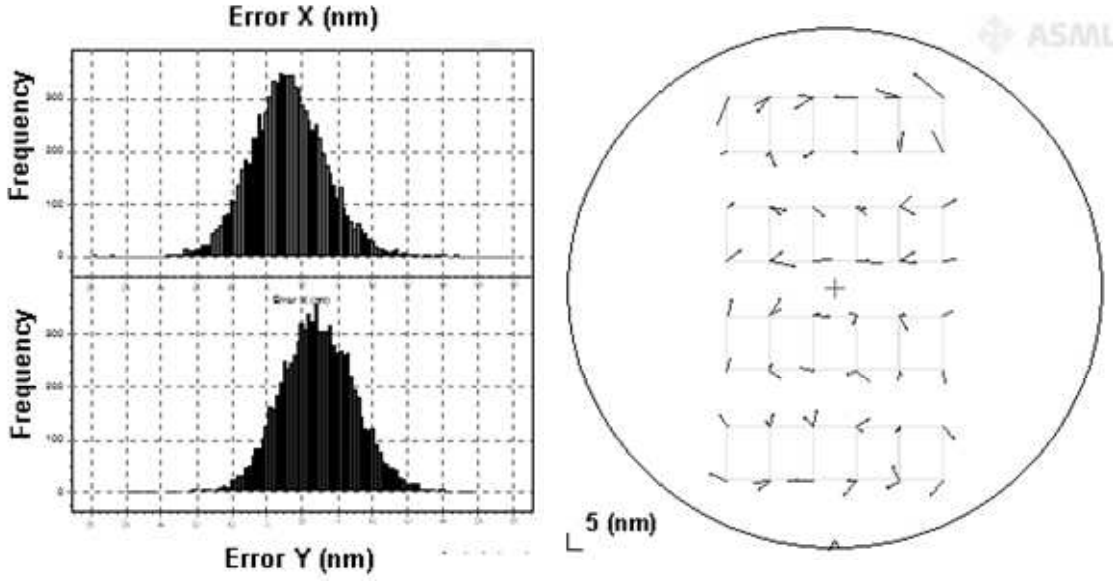
a)

Contact	Average CD	3σ
1	37.2 nm	4.1 nm
2	44.2 nm	4.0 nm

b)

Figure 3 – (a) SEM image of the contact level of a 80-nm pitch SRAM flycell printed in 100 nm thick film of SEVR-78 resist using single exposure EUV lithography. (b) CD control data for contact holes #1 and #2 at 18 mJ/cm^2 dose.

Champion multiple machine overlay results between the contact level patterned with single exposure EUV lithography and the previous layer patterned with 193 nm immersion lithography are shown in Figure 4. The mean overlay errors were 1.5 nm in x and 1.7 nm in y and the residual overlay errors were 8.0 in x and 7.8 nm in y. These errors are significantly higher than the best single machine overlay numbers for the Albany ADT (2.2 nm in x and 2.8 nm in y) but are well within the overlay specifications for the tool.[9]



a) b)

Figure 4 – (a) Single machine overlay data for the EUV Alpha Demo Tool in Albany. The champion, mean + 3σ overlay values were 2.2 nm in x and 2.8 nm in y. (b) Multiple machine overlay data for the contact layer printed with single exposure EUV lithography and the under laying active layer patterned with 193 nm immersion lithography. The mean errors were 1.5 nm in x and 1.7 nm in y and the residual overlay errors were 8.0 nm in x and 7.8 nm in y.

The fully-processed integrated device wafers required a large number of processing steps beyond the EUV imaging of the contact level pattern. First, the contact level EUV resist images were transferred into a silicon-containing BARC, then into an organic planarizing layer, and finally into an inter-level dielectric. Then, a novel Cu metallization scheme was used to fill the high-aspect-ratio contacts. Finally, a metal interconnect level was printed with double-dipole 193 nm immersion lithography, fabricated using a Cu damascene technique, and polished before electrical probing of the devices was carried out. A cross-sectional TEM through the fully-processed 0.076 μm^2 SRAM array is shown in Figure 5. The high-aspect-ratio contacts, tapering from ~37 nm diameter at the contact/interconnect interface to ~30 nm diameter when they come into contact with a source or a drain, are accurately positioned between the FinFETs. The fins are not visible in Figure 5 because they are oriented parallel to the plane of the figure and are located behind the row of contacts. The metal interconnects, which were patterned using double-dipole 193 nm immersion lithography, are visible in the top 25% of the figure. The slight misalignment of the metal interconnects with respect to the contacts is believed to have had little or no influence on the electrical performance of the devices.

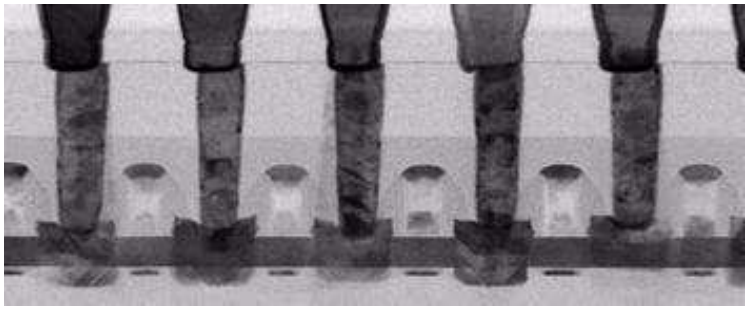


Figure 5 – Cross sectional TEM image of the fully-process 0.08 μm^2 6T-SRAM.

Butterfly curves for 0.076 μm^2 SRAM flycells in all 20 of the chips patterned at the contact level with single exposure EUV lithography and at the first interconnect level with double-dipole 193 nm immersion lithography are shown in Figure 6. Nearly 100% of the chips had functioning SRAM flycells and the SRAM flycells in the best chips exhibited a healthy static-noise-margin (SNM) of 148 mV at V_{dd} = 0.9 V.

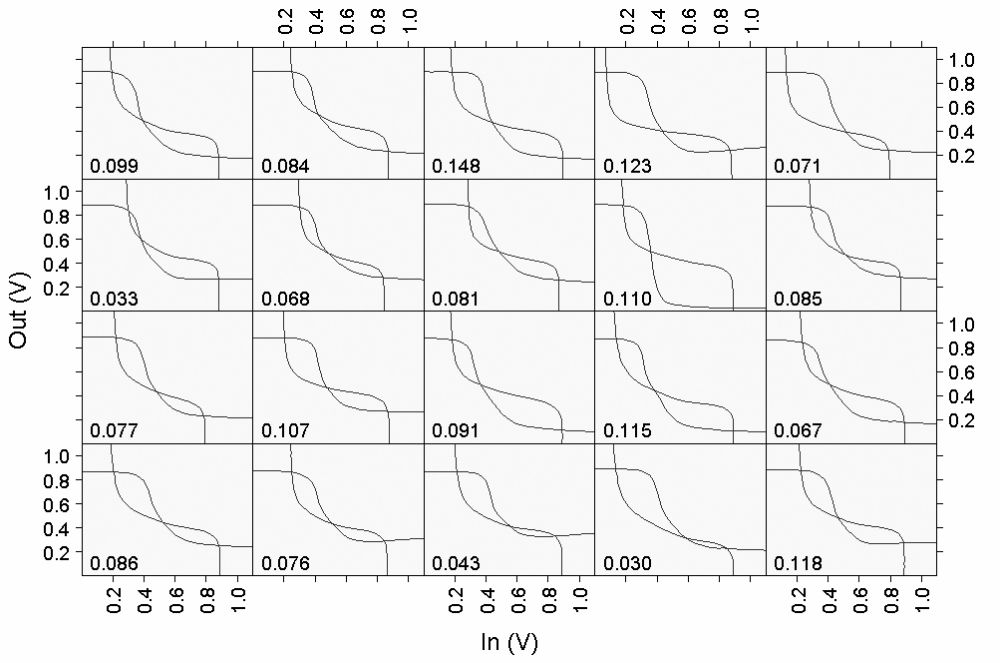


Figure 6 – Butterfly curves for the 0.076 μm^2 SRAM flycells in all 20 chips patterned at the contact level with single exposure EUV lithography and at the first interconnect level with double-dipole 193i immersion lithography.

3. 22-nm NODE TEST CHIPS WITH EUVL INTERCONNECT LEVEL

The layer structure of the 22-nm node test chips used for the EUV device demonstration work described in this section, in which the contact level was patterned with double exposure, double etch (DE^2) 193 nm immersion lithography, and the first interconnect level was patterned with single exposure EUV lithography, is illustrated in Figure 7.

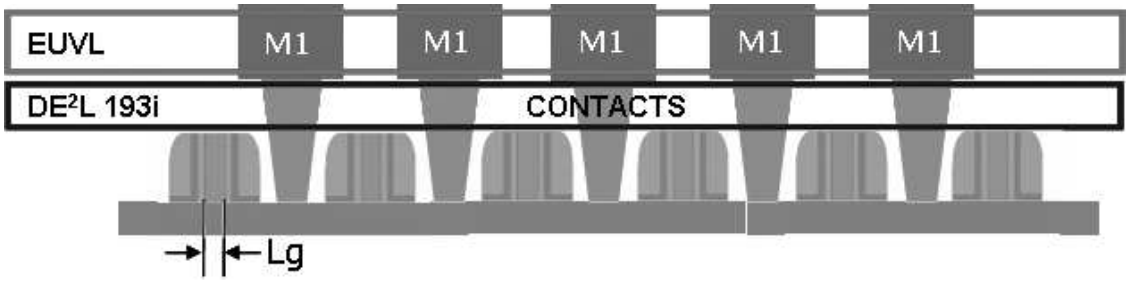


Figure 7 – Integrated stack of 22-nm node test chips in which the contact level was patterned with double-exposure double-etch 193 immersion lithography and the interconnect (M1) level was patterned with single exposure EUV lithography.

The mask data for the 22-nm interconnect level was corrected for conventional OPC and for mask shadowing, but not for imaging system flare because the density of the interconnect level is still sufficiently low (<30%). Model-based OPC was applied to the layout data using Mentor Graphics Calibre nmOPC. The interconnect level data was corrected for the mask shadow effect by making horizontal lines larger by 1.5 nm and vertical lines smaller by 1.5 nm. The corrected data was used by the AMTC to fabricate a 22- nm node interconnect level EUV mask using the same kind of blanks that were employed at the contact level. In this case, however, KLA-Tencor 5xx inspection of the interconnect-level mask found 1197 defects >60 nm in size. The larger defect density of the interconnect level mask was due, at least in part, to the larger open area in the interconnect patterns (~30%).

As was done with at the contact level, EUV lithography at the interconnect level was carried out using the ADT in Albany, New York. The resist used for interconnect level patterning was SEVR-139, which is available from Shin-Etsu MicroSci, Inc. A plot of printed CD (nm) versus exposure dose (mJ/cm^2) for 40 nm wide dense lines and spaces in a 75 nm thick film of SEVR-139 using the ADT is shown in Figure 8. At all EUV doses > 17.5 mJ/cm^2 (the dose range over which the resist is fully cleared), the horizontal-vertical print difference is less then 0.4 nm, showing that the shadow effect correction of the data for the interconnect level mask was nearly perfectly done.

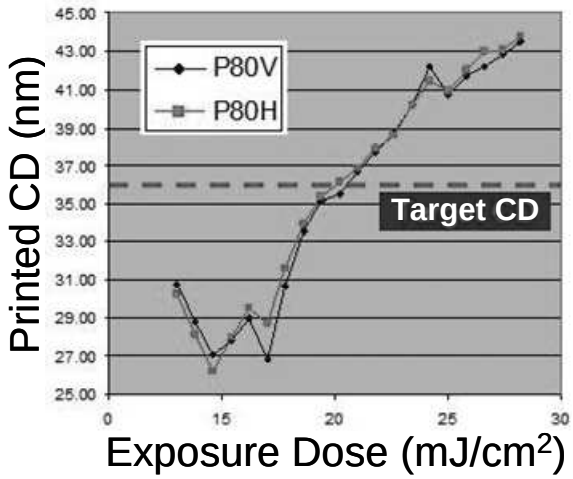
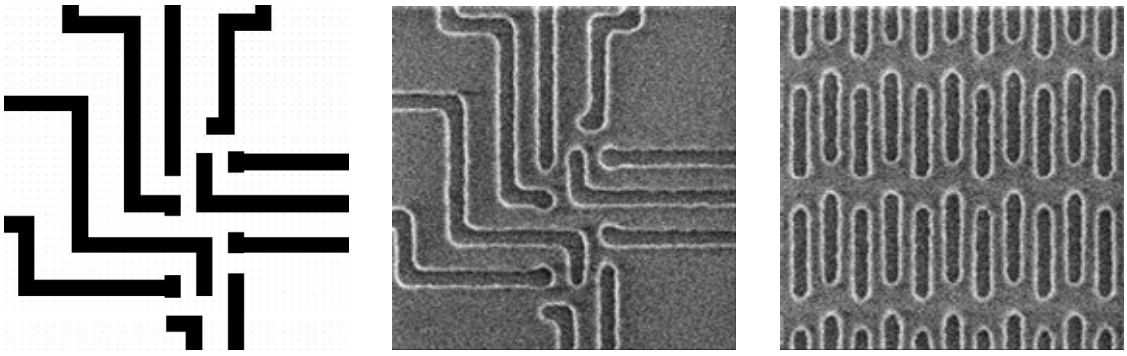


Figure 8 – CD data for imaging of 80-nm pitch line and space patterns in 75 nm thick films of SEVR-139 resist printed with EUV lithography showing that the mask shadow effect correction of the first interconnect level patterns was done nearly perfectly.

The quality of the EUV imaging of interconnect level patterns at the 22 nm node is illustrated in Figure 9. Figure 9(a) shows the layout for a 0.08 μm^2 6T-SRAM flycell. Figure 9(b) shows a top-down SEM image of the 0.08 μm^2 SRAM flycell layout in a 75 nm thick film of SEVR-139 produced with the ADT. The EUV resist image is a nearly perfect replica of the layout as would be expected given the high value of k_1 for EUV lithography at 80 nm pitch ($k_1 = 0.74$). Figure 9(c) shows an EUV image of an 80 nm pitch dense via chain pattern in a 75-nm thick layer of SEVR-139 resist with excellent line-end to line-end performance.



a) b) c)

Figure 9 – (a) 0.08 μm^2 SRAM flycell layout. (b) EUV images of 0.08 μm^2 SRAM flycell in 75 nm thickness of SEVR-139 resist. (c) EUV images of 80 nm pitch first interconnect level dense via chain patterns in 75 nm thick film of SEVR-139 resist.

Butterfly curves for the 0.094 μm^2 SRAM flycells in all 20 of the chips patterned at the contact level with DE^2 193 nm immersion lithography and at the interconnect level with single exposure EUV lithography are shown in Figure 10. In this case, only ~25% of the flycells were active with the best cell exhibiting a static-noise-margin of 131 mV at $V_{dd} = 0.9$ V. The reasons for the poorer electrical performance of the device patterned at the contact level with DE^2 193 nm immersion lithography and at the interconnected level with single exposure EUV lithography are not yet known. However, given the high quality of the EUV interconnect level images shown in Figure 9, unless the overlay errors with EUV lithography were extraordinarily high or the Cu deposition/CMP steps required at the interconnect level post EUV litho was substandard, then the patterning of the contact level with DE^2 193 nm immersion lithography is likely at fault.

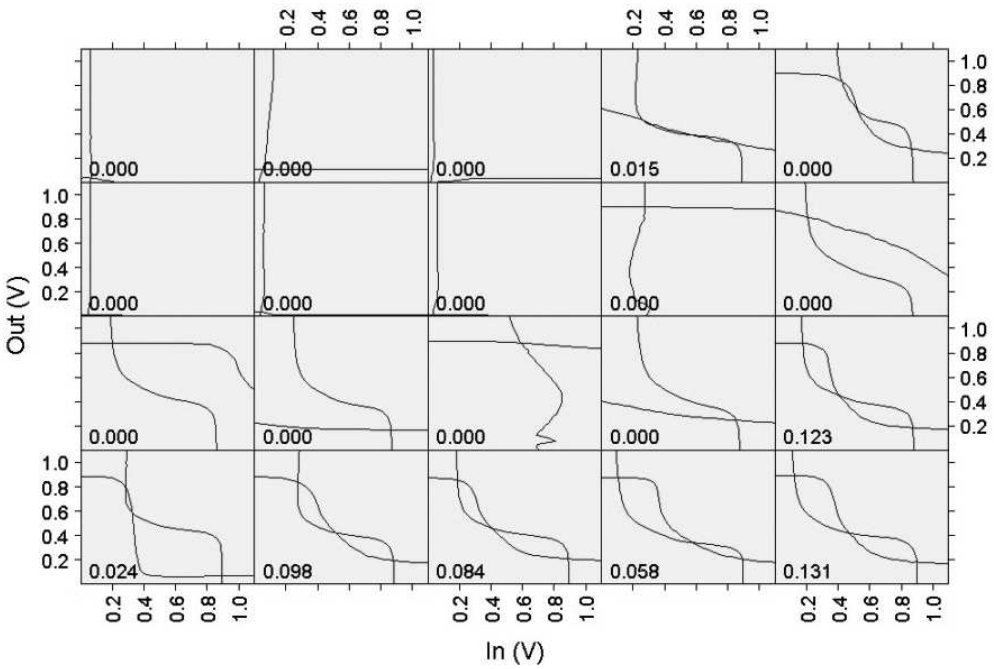
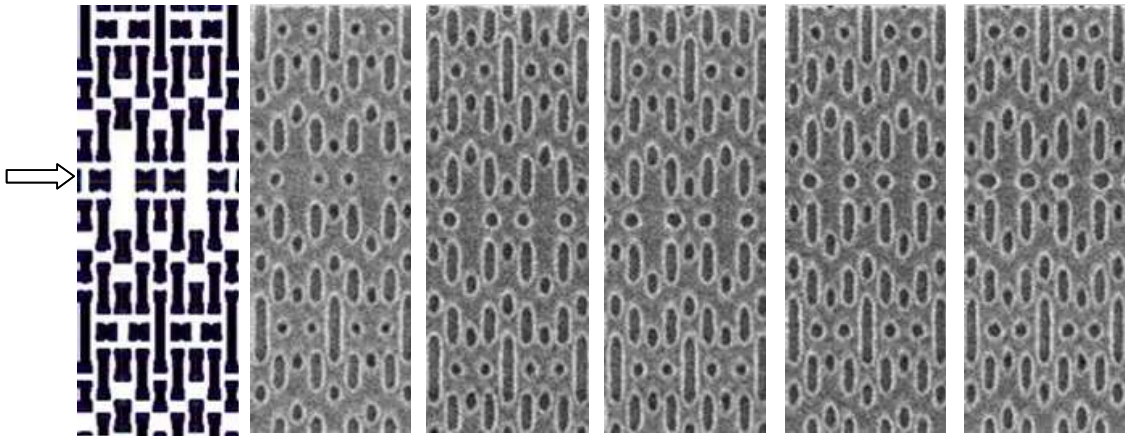


Figure 10 – Butterfly curves for 0.094 μm^2 SRAM cells patterned at the contact level with double-exposure double-etch 193 nm immersion lithography and at the first interconnect level with single exposure EUV lithography.

4. EUV OPTICAL PROXIMITY CORRECTION AT THE 15-nm NODE

EUV lithography with the 0.25 NA ADT appears to be capable of supporting some early device development work at the 15 nm technology node. Some preliminary results from the use of OPC to correct interconnect level patterns at 56 nm pitch are shown in Figure 11. Figure 11(a) shows a portion of the layout of an 80 nm pitch SRAM pattern at the interconnect level that has been scaled to 56 nm pitch and that has been corrected for the mask shadow effect. Figure 11(b) shows an image of the 56 nm SRAM pattern in a 75 nm thick film of SEVR-139 resist printed with the ADT. Clearly, the resist image in Figure 11(b) is a less than faithful replica of the layout; all of the trenches are foreshortened in their vertical dimension and the row of isolated contacts (marked with a horizontal arrow in Figure 11(a)) is grossly undersized. Figures 11(c) – 11(f) show EUV images of the 56 nm pitch SRAM pattern after correcting for the mask shadow effect and after OPC with increasing amounts of resist blur (0, 5, 10, & 20 nm) in 75 nm thick films of SEVR-139 resist. Clearly, the use of OPC has resulted in a greatly improved overlap between the process windows for the vertical trenches and the isolated contacts.



a) b) c) d) e) f)

Figure 11 – (a) 80 nm pitch M1 SRAM layout scaled to 56 nm pitch. (b) EUV resist image of 56 nm pitch M1 SRAM pattern corrected for the EUV mask shadow effect but without optical proximity correction. (c)–(f) EUV resist images of 56 nm pitch SRAM pattern corrected for the EUV mask shadow effect and for the optical proximity effect with increasing amount of resist blur.

5. CONCLUSIONS

EUV lithography with the 0.25 NA ADT has been used successfully to print the contact and interconnect levels on 22-nm node test chips. The quality of the printing at the 22-nm node is considerably higher than the printing produced with double-dipole or double-exposure, double-etch 193 nm immersion lithography and the device yield is also considerably higher. EUV printing with the 0.25 NA ADT is capable of supporting some early device development at the 15 nm technology node. Recent progress in EUV resist development has been outstanding and the performance of a few state-of-the-art EUV resists is already sufficient for 22-nm node pilot production[10]. Mask defectivity is now the most serious remaining EUV critical issue. Fortunately, the defect levels of the current best EUV mask banks are approaching those needed for masks to be used in pilot production at the 22-nm node, particularly for low pattern density levels.

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